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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): RFG.006CP1

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on February 19, 2007

Signature: [signature]

Typed or printed name: Robert F. Gazdzinski

Application Number	Filed
09/817,842	03/26/2001

First Named Inventor: Robert F. Gazdzinski

Art Unit	Examiner
3739	Leubecker

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [XX] attorney or agent of record. Registration number 39,990
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

[signature]
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February 19, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of _____ forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Robert F. Gazdzinski	Appl. No.:	09/817,842
Examiner:	Leubecker, John P.	Gr. Art Unit:	3739
Filing Date:	03/26/2001		
For:	**ENDOSCOPIC SMART PROBE AND METHOD**		

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

In reply to the Office Action dated October 19, 2006 ("Office Action"), Applicant herein requests a pre-appeal brief review of the above-identified application as follows:

I. CLEAR ERROR ON APPLICANT'S TEACHINGS AND DISCLOSURE

a) Per page 2, Par. 2 of the Office Action, the Examiner rejects Claim 16 as being indefinite under Section 112(2). The Examiner asserts that Applicant's use of "extension" is vague and indefinite.

The Examiner has seemingly neglected to review the references cited by Applicant and incorporated into its specification at time of filing, including *inter alia* U.S. Patent No. 6,065,027 entitled "Data Processor with Up Pointer Walk Trie Traversal Instruction Set Extension", which clearly and unambiguously discloses: (i) extension instructions (e.g., Col. 5, line 25) ; (ii) extension hardware (e.g., ALU or "XALU") (e.g., Col. 5, line 20); (iii) extension registers (e.g., Col. 15, line 57); (iv) extension processor instruction logic circuits (e.g., Col. 5, line 15). As is well known by those of ordinary skill in the art, the term "extensions" is a generic term that can refer to hardware, instructions, and even other types of facilities. Moreover, the different types of "extensions" are typically used with one another, as in the '027 patent. For the **Examiner to say that the term "extension" is unsupported or vague is therefore respectfully disingenuous, and comprises clear error.**

Regarding Claim 39, similar logic applies (note that a "software extension" clearly refers to a software-based extension of which an extension instruction is one particular species"). Applicant's disclosure clearly has support for at least one type of software extension (extension instruction), and hence is in no way vague or indefinite.

a) Per page 2, Par. 2 of the Office Action, the Examiner rejects Claim 36 as being indefinite under Section 112(2). The Examiner asserts that Applicant's use of "*substantially unique from any other code*" is indefinite.

The Examiner's assertions regarding "self-fulfillment" are respectfully misplaced and incorrect. In fact, spreading codes are not necessarily substantially unique, and in fact may even repeat across several different users. As a simple example, a frequency-hopping spread spectrum (FHSS) spreading code (hopping sequence) is typically generated using an algorithm which necessarily produces the same result when seeded with the same initial value. This is how the receiver can synchronize to the same sequence or code (i.e., it uses the same algorithm and the same seed). See, e.g., the well known GSM (Global System for Mobile Communications) which

uses such a code. Since the population of seeds in necessarily limited, even different users will sometimes generate the same sequence, just shifted in time.

Accordingly, Applicant submits that the Examiner's assertion is clear error, since at least one common instance of where spreading codes are not "substantially unique" has been presented.

II. CLEAR ERROR ON CASE LAW AND INTERPRETATION OF APPLICANT'S CLAIMS

Per page 3, Par. 3 of the Office Action ("Note"), the Examiner asserts that Applicant's claims 16, 39, 40, 52, and 53 are "product by process" or contain process limitations that should be given no patentable weight.

Applicant notes that Examiner has seemingly taken any verb present in Applicant's claim 16 to label the entire claim as "product by process", and therefore discount the structural or non-process limitations present therein. For example, regarding Claim 16, Applicant notes that the highlighted portions presented below are purely structural in nature:

> *16. (Previously presented) The probe of Claim 15,* ***wherein said data processor comprises at least a processor core optimized for power consumption****, said optimization comprising selecting* ***a processor core configuration including at least one extension that satisfies a target core speed criterion while minimizing gate count.***

Instead, however, the Examiner completely and improperly ignores these limitations under the rubric of "they're all process-related" (paraphrasing). Neither Brune nor Alfano nor Banyai teach or suggest anything that Applicant can find regarding "power consumption optimization". Note that if one merely leaves the word "selecting" out of Claim 16, it is **completely structural in nature**.

Accordingly, the Examiner not only erroneously failed to address the structural limitations in Claim 16, but has also failed to provide any citation in any of his referenced art that teach or suggest such limitations. Accordingly, this comprises clear error.

III. CLEAR ERROR OF WHAT ALFANO TEACHES

a) In furtherance of the discussion presented above under Item II., Applicant notes that even if only the limitation "***wherein said data processor comprises at least a processor core optimized for power consumption...***" is read into Claim 16 (i.e., just removing any subsequent verbage from Claim 16), Alfano still in no way teaches or suggests such limitations. Applicant notes that it cannot find any teaching or even remote suggestion in Alfano that its processor is in any way optimized for or remotely considers power consumption in any way. The Examiner therefore does not meet his burden under Section 102; i.e., that each and every limitation be taught explicitly or by inherency. This rejection is therefore clear error.

b) Regarding Claim 35, Applicant requests the Examiner to point out where Alfano teaches or remotely suggests minimizing interference with other communication devices operated proximate said probe, as recited in Claim 35. The short answer is that it does not, and hence the Examiner's assertions are improper and comprise clear error since no teaching is present explicitly or by inherency.

Applicant further notes Par. 8 of the January 12, 2006 Office Action referenced by the Examiner; **note that this paragraph completely glosses over this limitation of Claim 35 (i.e., no discussion regarding communication interference is even attempted by the Examiner).**

c) Regarding Claim 38 - 41, Applicant requests the Examiner to point out where Alfano teaches or remotely suggests a data processor is designed so as to specifically consider both die size and power consumption for a given processor speed through at least elimination of gates that would otherwise be present but for said design considerations, as recited in Claim 38. Applicant's claim recites a processor specifically designed for the intended application (i.e., achieving a target speed while considering die size and gate count (proportional to power consumption). Alfano merely teaches that a processor can be placed on a semiconductor. **How is this even remotely anticipatory of the aforementioned specifically designed processor?**

Again, it is not, and hence the Examiner's rejection comprises clear error.

d) Regarding Claim 46, Applicant requests the Examiner to point out where Alfano teaches or remotely suggests data processor comprising at least one instruction particularly adapted for performing mathematical operations necessary for processing of data from said at least one image sensor, as recited in Claim 46. The short answer is that it does not; Alfano is completely silent on any type of instructions for its processor (and even the type or design of the processor itself. No details of any kind are provided). Hence, the Examiner's assertions are improper and comprise clear error since no teaching is present explicitly or by inherency.

Applicant further notes Par. 8 of the January 12, 2006 Office Action referenced by the Examiner; **note that this paragraph completely glosses over this limitation of Claim 46 (i.e., the Examiner merely states in effect that "a processor has instructions and mathematical operations"; no attempt to state that these instructions are particularly adapted for image sensor data processing as recited in Claim 46 is made).**

Similar logic Applies to Claims 50-53; however, this is an even more egregious case, since independent Claim 50 recites at least one instruction particularly adapted for performing mathematical operations necessary for processing data from said at least one image sensor for transmission over said at least one interface. Hence, Claim 53 goes even further than Claim 46, **and requires that the adaptation of the instruction be for purposes of transmission over said interface** (e.g., a FFT butterfly, CRC, etc; see page 50 of Applicant's specification). This is in no way taught or remotely suggested by Alfano.

IV. CLEAR ERROR OF WHAT BRUNE TEACHES

The Examiner states on page 3-4 of the Office Action (relating to Claims 35, 38-41, 46, 48 and 50) that he "*still takes the position that the circuit board of Brune, which is in part semi-conductive by nature, and is die-like (flat, wafer shaped) in shape, meets the limitations of a single semi-conductive die...*"

a) **A circuit board is not a semiconductor** - Brune in no way that Applicant can find even remotely teaches or suggests a semiconductive die (i.e., a piece of a semiconductive wafer or the like), as recited in Applicant's Claims 15 and 40. Applicant traverses this rejection in its entirety, and submits that it is clear error.

The Examiner respectfully has conveniently left the word "*semi*" off of the recited limitation of "single semiconductive die" (see page 4, line 6, Par. 7 of the January 2006 Office Action); Brune in no way teaches or suggests a single **semi**conductive die for the processor and communications device.

Also, how is a circuit board "in part, semi-conductive by nature" as asserted by the Examiner on page 4 of the October 2006 Office Action? **Is the Examiner stating that a circuit board is semi-conductive by nature because it has a semiconductor mounted on it? This is respectfully ludicrous.** The Examiner cannot claim inherent teaching, and hence the Section 102 rejection is improper.

Furthermore, a circuit board is not a **die** (the term "die" being well known to those of ordinary skill in the integrated circuit arts, especially when interpreted in light of Applicant's detailed specification, as being a single piece of semiconductive material (e.g., silicon, GaAs, SiGe, etc.). Where does Brune even remotely teach this? **It does not, and hence Brune cannot support an anticipation rejection, since it fails to teach every element explicitly or by inherency.**

b) **Evidence of Non-obviousness Ignored** - Moreover, with respect to any obviousness rejection (see Par. 8 of the October 2006 Office Action), Brune's teaching of a circuit board (i.e., board level) electronics teaches away from use in a human being as now recited in Claim 15, since a board as described by Brune simply would not fit within a human intestinal tract (especially along with the remaining components recited in Applicant's claimed inventions) unless properly miniaturized. Brune makes no teaching or suggestion of (i) such miniaturization, or (ii) use of his invention in a human being.

Similarly, Applicant also notes that *"[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the 'subject matter as a whole' which should always be considered in determining the obviousness of an invention under 35 U.S.C. § 103."* In re Sponnoble, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969). See MPEP 2141.02; "*The court found the inventor discovered the cause of moisture transmission was through the center plug, and there was no teaching in the prior art which would suggest the necessity of selecting applicant's plug material which was more impervious to liquids than the natural rubber plug of the prior art.*" **Brune**

does not in any way demonstrate an appreciation of the problem solved by Applicant's claimed invention; i.e., reduction in physical size and power consumption so that the recited apparatus can be used in a human being.

Hence, the Examiner's failure to consider this teaching away and non-obviousness evidence is a second, distinct basis for clear error.

V. CLEAR ERROR – "HOUSE OF CARDS"

Applicant lastly notes and traverses the Examiner's rejections of claims which depend directly or indirectly on any of the claims previously discussed herein. Based on the foregoing, each of the bases of rejection for the previously discussed claims is clearly erroneous, and hence the Examiner's rejections of further depending claims are, respectfully, necessarily built on a house of cards. Specifically, not each and every element of each of these dependent claims is taught or suggested by the references cited by the Examiner.

As one specific example, consider the fact that **neither Brune nor Alfano nor Banyai nor Kratz nor Soussi nor Roberts teach or suggest anything that Applicant can find regarding "power consumption optimization". Hence, Claims 17, 18, 19, 20, 21, 22, 23, 24, 25, and 26, which all depend directly or indirectly from Claim 16, are necessarily not anticipated or obvious based on the art cited by the Examiner.**

Summary

Applicant has herein respectfully provided at least one bases, and in many cases two or more bases, for overturning the Examiner's Section 112, 102 and/or 103 rejections of numerous now pending claims based on clear error. Accordingly, Applicant requests that these claims be allowed at the earliest opportunity.